

(15)

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: Phuongchau Nguyen Examiner #: 75852 Date: 11/17/03Art Unit: 2665 Phone Number 305-10093 Serial Number: 09/469,979Mail Box and Bldg/Rm Location: CPK2-3A 2-3 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

***** Please provide a detailed statement of the search topic; and describe as specifically as possible the subject matter to be searched.

Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples of relevant citations, authors, etc., if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Apparatus and Method for converting data in serial format to parallelInventors (please provide full names): JONAS ALLOEER SKOU; BERTIL ROSTLUND, and vice versaPATRIK SUNSTRÖMEarliest Priority Filing Date: 12/28/98 (Dec 28, 98)

For Sequence Searches Only Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.

→ Bus, (serial and parallel) same (converting or conversion)
 → Buffer & same (divide & 3 or separate & 3 or demultiplex & 3), with
 (★) Bus same portions
 3 -> (array with (memory or storage or buffer)) same (part #)
 4 -> operation with max 2 and predetermined cycle
 sequential and simultaneously
 ⇒ Please see claim with keywords (BOLD)
 See bolded words attached

★ = mean important

11-7-03

STAFF USE ONLY

Type of Search

Vendors and cost where applicable

Searcher: Pamela ReynoldsNA Sequence (#): 24

STN

Searcher Phone #: 305-1025AA Sequence (#): 24

Dialog

Searcher Location: PLC 23 C03Structure (#): 330

Questel/Orbit

Date Searcher Picked Up: 7-17-03

Bibliographic

Dr. Link

Date Completed: 11-17

Litigation

Lexis/Nexis

Searcher Prep & Review Time: 7M

Fulltext

Sequence Systems

Clerical Prep Time:

Patent Family

WWW/Internet

Online Time:

Other

Other (specify)



STIC Search Report

EIC 2600

STIC Database Tracking Number: 107940

TO: Phuongchau Nguyen

Location: PK2 3A23

Art Unit: 2665

Monday, November 17, 2003

Case Serial Number: 09469979

From: Pamela Reynolds

Location: EIC 2600

PK2-3C03

Phone: 306-0255

Pamela.Reynolds@uspto.gov

Search Notes

Dear Phuongchau Nguyen,

Please find attached the search results for 09469979. I used the search strategy I emailed to you to edit, not hearing from you I proceeded. I searched the standard Dialog files, IBM TDBs, the wayback machine, and the internet.

If you would like a re-focus please let me know.

Thank you.

Pamela Reynolds



File 2:INSPEC 1969-2003/Nov W2
(c) 2003 Institution of Electrical Engineers
File 6:NTIS 1964-2003/Nov W3
(c) 2003 NTIS, Intl Cpyright All Rights Res
File 8:Ei Compendex(R) 1970-2003/Nov W2
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File 35:Dissertation Abs Online 1861-2003/Oct
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File 94:JICST-EPlus 1985-2003/Nov W3
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File 95:TEME-Technology & Management 1989-2003/Oct W4
(c) 2003 FIZ TECHNIK
File 99:Wilson Appl. Sci & Tech Abs 1983-2003/Oct
(c) 2003 The HW Wilson Co.
File 144:Pascal 1973-2003/Nov W2
(c) 2003 INIST/CNRS
File 233:Internet & Personal Comp. Abs. 1981-2003/Jul
(c) 2003, EBSCO Pub.
File 239:Mathsci 1940-2003/Dec
(c) 2003 American Mathematical Society
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
(c) 2002 The Gale Group
File 603:Newspaper Abstracts 1984-1988
(c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2003/Nov 15
(c) 2003 ProQuest Info&Learning

? ds

Set Items Description
S1 25470 (CONVERT? OR CONVERS? OR CHANG? OR MODIF? OR ADJUST? OR AL-
TER?) AND BUS
S2 266 S1 AND SERIAL AND PARALLEL
S3 3667 S1 AND (PARTITION? OR DIVID? OR SEPERAT? OR DIVISION? OR P-
ART OR PARTS OR SECTION?? OR SEGMENT?? OR PORTION?? OR FRAGME-
NT? OR PIECES OR SECTOR??)
S4 1433 ARRAY? AND (MEMORY OR BUFFER?? OR STORAGE OR STORAGE(3N)CE-
LLS) AND PORT??
S5 4 (ONE OR SINGLE OR 1)(BUFFER?(3N)ELEMENT??
S6 159 CLOCK AND (CONTROL OR MONITOR OR DIRECT?) AND ACCESS??? AND
(SEQUENTIAL? OR SIMULTANEOUS? OR CONCURRENT? OR COINCIDENT?)
S7 1869 (WRITE OR READ)(3N)CYCLE??
S8 122 AU=(ALOWERSSON, J? OR ROSLUND, B? OR SUNDSTROM, P? OR ALO-
WERSSON J? OR ROSLUND B? OR SUNDSTROM P?)
S9 9463 (PRESELECT? OR (PRE()(SELECT? OR SET OR DETERMIN? OR SELEC-
T? OR SPECIFIED) OR PREDETERMIN? OR SPECIFIC OR SPECIFIED OR -
SET OR PRESET))(3N)CYCLE?
S10 3 S2 AND S4
S11 1 RD S10 (unique items)
S12 4 S5 NOT S10
S13 3 RD S12 (unique items)

S14 2 S6 AND S7
S15 2 S14 NOT (S5 OR S10)
S16 1075 S3 AND DATA
S17 0 S2 AND S6
S18 1 S2 AND S7
S19 1 S18 NOT (S14 OR S5 OR S10)
S20 0 S8 AND S1
S21 0 S8 AND S9
S22 0 S4 AND S8
S23 5 S3 AND S4
S24 5 S23 NOT (S18 OR S14 OR S5 OR S10)
S25 4 RD S24 (unique items)

11/3,K/1 (Item 1 from file: 2)

DIALOG(R) File 2:INSPEC

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7702978 INSPEC Abstract Number: A2003-18-4240J-002, B2003-09-4350-014,
C2003-09-5120-007

Title: Using field programmable gate arrays to scale up the speed of
holographic video computation

Author(s): Nwodoh, T.A.

Author Affiliation: Media Lab., MIT, Cambridge, MA, USA

Journal: Journal of Electronic Imaging vol.12, no.3 p.558-66

Publisher: SPIE-Int. Soc. Opt. Eng,

Publication Date: July 2003 Country of Publication: USA

CODEN: JEIMES ISSN: 1017-9909

SICI: 1017-9909(200307)12:3L.558:UFPG;1-B

Material Identity Number: P618-2003-003

U.S. Copyright Clearance Center Code: 1017-9909/2003/\$15.00

Language: English

Subfile: A B C

Copyright 2003, IEE

Title: Using field programmable gate arrays to scale up the speed of
holographic video computation

...Abstract: of the VCCs. The VCC formats compute holographic data from
multiple hologram computing processor cards, converting the digital data
to analog form to feed the acousto-optic modulators of the Media...

... from the 3-D numerical description of a scene takes place inside
field-programmable gate arrays (FPGAs) resident in the processor card.
These large FPGAs employ several superposition processing pipelines, all
working in parallel to generate the fringes of the hologram frame. With
nine processor boards, there are the...

... also be loaded into the VCC from a host computer through the low-speed
universal serial bus (USB) port .

Descriptors: buffer storage ; ...

...field programmable gate arrays ; ...

... parallel processing

Identifiers: field programmable gate arrays ; ...

... parallel processing...

...universal serial bus port ; ...

...USB port

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13/3,K/1 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

5690563 INSPEC Abstract Number: B9710-6230B-010

Title: A 622 Mb/s 32*32 scalable shared buffer ATM switch with searchable address queue

Author(s): Saito, H.; Kondoh, H.; Yamanaka, H.; Sasaki, Y.; Tsuzuki, M.; Kohama, S.; Yamada, H.; Matsuda, Y.; Oshima, K.

Author Affiliation: Inf. Technol. R&D Center, Mitsubishi Electr. Corp., Kanagawa, Japan

Conference Title: IEEE GLOBECOM 1996. Communications: The Key to Global Prosperity. Conference Record (Cat. No.96CH35942) Part vol.2 p.1363-8 vol.2

Publisher: IEEE, New York, NY, USA

Publication Date: 1996 Country of Publication: USA 3 vol. (xvi+xxxiii+xvii+2169) pp.

ISBN: 0 7803 3336 5 Material Identity Number: XX97-00868

U.S. Copyright Clearance Center Code: 0 7803 3336 5/96/\$5.00

Conference Title: Proceedings of GLOBECOM'96. 1996 IEEE Global Telecommunications Conference

Conference Sponsor: IEEE Commun. Soc.; IEE; UKRI Commun. Chapter; BT; FUJITSU; ALCATEL Telecom; Braodband Technol.; NORTEL Northern Telecom; Lucent Technol.; ERICSSON

Conference Date: 18-22 Nov. 1996 Conference Location: London, UK

Language: English

Subfile: B

Copyright 1997, IEE

...Abstract: architecture and the searchable address queuing scheme, is described. A 622 Mb/s 32*8 element switch consists of one buffer LSI and one control LSI. A 622 Mb/s 32*32 switch which comprises four...

13/3,K/2 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

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5079783 INSPEC Abstract Number: B9511-6150C-077, C9511-3370-024

Title: Analysis and simulation of the buffered-expanded delta fast packet switch

Author(s): Awdeh, R.Y.; Mouftah, H.T.

Author Affiliation: Dept. of Electr. & Comput. Eng., Queen's Univ., Kingston, Ont., Canada

Conference Title: 1994 IEEE GLOBECOM. Communications: The Global Bridge. Conference Record (Cat. No.94CH34025) Part vol.1 p.470-4 vol.1

Publisher: IEEE, New York, NY, USA

Publication Date: 1994 Country of Publication: USA 3 vol. xxvi+1957 pp.

ISBN: 0 7803 1820 X

U.S. Copyright Clearance Center Code: 0 7803 1820 X/94/\$4.00

Conference Title: 1994 IEEE GLOBECOM. Communications: The Global Bridge

Conference Sponsor: IEEE Commun. Soc.; IEEE San Francisco Sect.; Alcatel Network Syst.; Digital Switch Corp.; Electrohome; Hewlett-Packard Lab.; Pacific Bell; Sprint; Sun Microsyst.; Tellabs Oper.; Texas Instrum.; Northern Telecom; AT&T Network Syst.; Bechtel; NEC America; Pirelli Corp

Conference Date: 28 Nov.-2 Dec. 1994 Conference Location: San Francisco, CA, USA

Language: English

Subfile: B C

Copyright 1995, IEE

...Abstract: achieve high performance is significantly reduced. In particular, an L of 4 combined with a **single buffer** at each switching **element** inlet results in above 95% maximum throughput for a very large-size switch. Finally, the...

13/3,K/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04704121 E.I. No: EIP97053667058

Title: 622 Mb/s 32 multiplied by 32 scalable shared buffer ATM switch with searchable address queue

Author: Saito, H.; Kondoh, H.; Yamanaka, H.; Sasaki, Y.; Tsuzuki, M.; Kohama, S.; Yamada, H.; Matsuda, Y.; Oshima, K.

Corporate Source: Mitsubishi Electric Corp, Kamakura, Jpn

Conference Title: Proceedings of the 1996 IEEE Global Telecommunications Conference. Part 2 (of 4)

Conference Location: London, UK Conference Date: 19961118-19961122

E.I. Conference No.: 46413

Source: Conference Record / IEEE Global Telecommunications Conference v 2 1996. IEEE, Piscataway, NJ, USA, 96CH35942. p 1363-1368

Publication Year: 1996

CODEN: CRIEET

Language: English

...Abstract: the searchable address queueing scheme, is described. A 622 Mb/s 32 multiplied by 8 **element** switch consists of **one Buffer** LSI and one Control LSI. A 622 Mb/s 32 multiplied by 32 switch which...
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19/3,K/1 (Item 1 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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02107069 E.I. Monthly No: EIM8607-049519

Title: VLSI SYSTEM FOR MULTIPROCESSOR INTERCONNECTION.

Author: Arden, Bruce W.; Ginosar, Ran; Schwartz, Avi

Corporate Source: Princeton Univ, Princeton, NJ, USA

Conference Title: Proceedings - IEEE 14th Convention of Electrical & Electronics Engineers in Israel.

Conference Location: Tel Aviv, Isr Conference Date: 19850326

E.I. Conference No.: 07919

Source: Proceedings - IEEE Convention of Electrical & Electronics Engineers in Israel 14th. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 85CH2075-0), Piscataway, NJ, USA Pap 4. 2. 1, 4p

Publication Year: 1985

CODEN: PCEIEP

Language: English

Abstract: An interconnection with switching chip for shared memory multiprocessor system is proposed. The **parallel** busses of many processors and memory modules are **converted** to **serial** links, enabling one chip to fully connect reasonably many of them (64 or more). Internal...

...number of processors, whereas the system cost is orders of magnitude smaller than that of **parallel** interconnections, e. g. multistage alignment networks. (Author abstract) 2 refs.

Identifiers: DATA BUS ; WRITE CYCLE ; READ CYCLE ; CHIP ARCHITECTURE

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25/3,K/1 (Item 1 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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06149073 E.I. No: EIP02397114142

Title: Parallel hardware architecture for CCD-mosaic digital mammography
Author: Smith, Scott T.; Kim, Hyunkeun; Swarnakar, Vivek; Jeong, Myoungki
; Wobschall, Darold C.

Corporate Source: Sensor Plus Inc., Amherst, NY 14226, United States

Conference Title: Medical Imaging 1998: Image Display

Conference Location: San Diego, CA, United States Conference Date:
19980222-19980224

E.I. Conference No.: 59761

Source: Proceedings of SPIE - The International Society for Optical Engineering v 3335 1998. p 663-674

Publication Year: 1998

CODEN: PSISDG ISSN: 0277-786X

Language: English

...Abstract: mammography has been accomplished. This paper presents this architecture including both the analog and digital **portions** of the imaging hardware. A two dimensional **array** of CCD sensors are used to capture the mammographic image synchronously and simultaneously. Each CCD's analog signal is **converted** to a 12 bits/pixel digital value through an **array** of high speed analog-to-digital **converters**. A parallel **array** of mesh connected TMS320C40 DSP processors then takes in the digital image data simultaneously. The...

...transport to the viewing workstation. One master DSP is located on the workstation's PCI **bus** which controls the parallel DSP **array** and collects compressed image data through a 60MB/s **port**. Since all computations are performed in parallel using local **memory** on each DSP, the overall acquisition, image registration, and transmission to display of the final...

Descriptors: Mammography; Charge coupled devices; Sensors; Digital signal processing; Analog to digital **conversion**; Image processing; Medical imaging; Parallel processing systems; Computation theory

25/3,K/2 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

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01301732 Genuine Article#: GM532 No. References: 0

Title: HIGH-SPEED AND CONTINUOUS RANGEFINDING SYSTEM

Author(s): ARAKI K; SATO M; NODA T; CHIBA Y; SHIMIZU M

Corporate Source: CHUKYO UNIV, SCH COMP & COGNIT SCI/TOYOTA 47003//JAPAN/

Journal: IEICE TRANSACTIONS ON COMMUNICATIONS ELECTRONICS INFORMATION AND SYSTEMS, 1991, V74, N10, P3400-3406

Language: ENGLISH Document Type: ARTICLE (Abstract Available) (NO REFS KEYED)

...Abstract: system-high speed and continuous measurement-mainly come from its image plane constructed by PSD **array** which is horizontally non-**divided** and linear, whereas vertically **divided** in numbers. Each row PSD element is attached to respective analog signal processor, A/D **converter** and **memory** element. By the virtue of this configuration of the image plane, we can store the positional information of slit-like image on the image plane into **memory** elements in real time, without waiting for one frame interval as is required in the...

...of the slit-ray from scanning time of it, which is set on the address bus of **memory** elements in our system. Thus, basic datum for 3-D measurement are acquired during only one scanning of slit-ray at high speed in the form of addresses of **memory** elements and datum stored in them. Moreover, if we use large capacity and/or dual **port** memories, we may continuously obtain 3-D datum of as many scenes as we want...

25/3,K/3 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-EPlus

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01417691 JICST ACCESSION NUMBER: 91A0908238 FILE SEGMENT: JICST-E
Special Issue on Computer Vision and Its Applications. High Speed and
Continuous Rangefinding System.
ARAKI K (1); SHIMIZU M (1); SATO M (2); NODA T (2); CHIBA Y (2)
(1) Chukyo Univ., Toyota-shi, JPN; (2) Nagoya Inst. Technology, Nagoya-shi,
JPN
IEICE Trans(Inst Electron Inf Commun Eng), 1991, VOL.E74, NO.10,
PAGE.3400-3406, FIG.13, REF.12
JOURNAL NUMBER: F0699BCQ ISSN NO: 0917-1673
UNIVERSAL DECIMAL CLASSIFICATION: 531.71/.74
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

...ABSTRACT: system-high speed and continuous measurement-mainly come from its image plane constructed by PSD **array** which is horizontally non-divided and linear, whereas vertically divided in numbers. Each row PSD element is attached to respective analog signal processor, A/D converter and **memory** element. By the virtue of this configuration of the image plane, we can store the positional information of slit-like image on the image plane into **memory** elements in real time, without waiting for one frame interval as is required in the...

...of the slit-ray from scanning time of it, which is set on the address bus of **memory** elements in our system. Thus, basic datum for 3-D measurement are acquired during only one scanning of slit-ray at high speed in the form of addresses of **memory** elements and datum stored in them. Moreover, if we use large capacity and/or dual **port** memories, we may continuously obtain 3-D datum of as many scenes as we want...

...DESCRIPTORS: AD conversion ;

...BROADER DESCRIPTORS: signal conversion ; ...

...transformation and conversion ;

25/3,K/4 (Item 1 from file: 144)

DIALOG(R)File 144:Pascal

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14530555 PASCAL No.: 00-0195296

1-V, 10-MHz, 3.5-mW, 1-Mb MTMOS SRAM with charge-recycling input/output buffers

SHIBATA N; MORIMURA H; WATANABE M

NTT System Electronics Lab, Kanagawa, Japan

Journal: IEEE Journal of Solid-State Circuits, 1999, 34 (6) 866-877

Language: English

...V, 10-MHz, 3.5-mW, 1-Mb MTCMOS SRAM with charge-recycling input/output buffers

... portable equipment, which is operated by a single battery cell of around 1 V. Its **memory** cells are made up of high-threshold-voltage (high-V_{th}) MOSFET's in order to...

... time can be predicted. Low-V_{th} MOSFET's are assigned for the critical paths of **memory** -cell access. The leakage current in each logic gate is reduced by high-V_{th} MOSFET...

... wordline scheme suitable for current-sense readout and a new half-swing bidirectional double-rail **bus** are used. The data-writing time is halved by means of a pulse-reset wordline architecture. To reduce the power dissipation, a 32- **divided memory array** structure is employed with a new redundant address-decoding scheme. Also, data transition detectors and a charge-recycling technique are employed for reducing the power dissipation of data-I/O **buffers**. A 64-K-words x 16-bits SRAM test chip, which was fabricated with a...

...is 1.2 μ W, and that at a 10-MHz read operation with the **modified** checkerboard test pattern is 3.9 mW for 30-pF loads.

English Descriptors: Multithreshold voltage; Charge recycling technique; Data transition detectors; Input output **buffers**; **Memory** cells; Theory ; CMOS integrated circuits; Threshold voltage; **Buffer storage**; Nickel cadmium batteries; MOSFET devices; Leakage currents; Logic gates; Integrated circuit testing; Electric power supplies to apparatus; Random access **storage**

French Descriptors: Theorie; Circuit integre CMOS; Tension seuil; Memoire tampon; Batterie nickel cadmium; Transistor MOS; Courant fuite; **Porte** logique; Essai circuit integre; Alimentation electrique appareil; Memoire acces direct

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